

# 17.5 A 5.4GHz 0.35µm BiCMOS FBAR Resonator Oscillator in Above-IC Technology

Mohammed Aissi<sup>1</sup>, Eric Tournier<sup>1</sup>, Marc-Alexandre Dubois<sup>2</sup>, Guy Parat<sup>3</sup>, Robert Plana<sup>1</sup>

<sup>1</sup>LAAS-CNRS, Toulouse, France

<sup>2</sup>CSEM, Neuchâtel, Switzerland

<sup>3</sup>CEA-LETI, Grenoble, France

Recently, significant efforts have been made to develop RF SoCs. The main challenge has been the integration of the high-Q RF filters, PLL reference oscillator, and the RF oscillator in some applications where the phase noise requirement is very stringent. The limitation is the low Q factor of the integrated passive devices due to the losses in the metallic interconnections and in the low resistivity substrate used in CMOS or BiCMOS processes. The thin film BAW resonators based on piezoelectric material, generally AlN or ZnO sandwiched between two metallic electrodes, have high Q, can handle high power and can operate at high frequencies (up to 16GHz). In addition, they have a small size and their fabrication in both configurations, film bulk acoustic wave resonator (FBAR) and solidly mounted resonator (SMR), is compatible with standard IC processes. For example, [1, 2] demonstrated the integration of the SMR and FBAR Filters above the RF IC substrate, respectively. Oscillators using FBAR and SMR resonators are also presented in [3, 4]. However, in both cases, the resonator is realized separately and wire bonded to the IC circuit. In this paper, a 5GHz FBAR based resonator oscillator where the FBAR is directly integrated above the IC is presented. The circuit was implemented in an AMIS 0.35µm SiGe BiCMOS process. Post processing directly the FBAR over the IC eliminates the parasitic and the modeling issue associated with the bondwire and reduces the circuit area. The oscillator is based on the Colpitts configuration and achieves a phase noise performance of -117.7dBc/Hz at 100kHz offset from the 5.46GHz carrier frequency.

The schematic of the oscillator and its equivalent circuit used for the analysis [5] are shown in Figures 17.5.1 and 17.5.2, respectively. The common collector transistor with the feedback capacitor  $C_1$  and  $C_2$  provide a negative resistance to compensate the losses in the FBAR resonator. This negative resistance is given by

$$R_n = -g_m / C_1 C_2 \omega^2 \quad (1)$$

where  $g_m$  is the transconductance of the transistor  $T_1$  and  $\omega$  is the frequency. To isolate the resonator from a 50Ω input impedance of the measurement instrument, the buffer transistor  $T_2$  is used. To minimize further loading of the resonator by the buffer, the output is tapped from the emitter of  $T_1$  via a small coupling capacitor  $C_c$ . The effective resistance  $R_e$  of the loaded resonator is given by

$$R_e = R_s + R_m (1 + C_0 / C_L)^2 \quad (2)$$

where  $C_L = (C_1 + C_\pi) C_2 / (C_1 + C_2 + C_\pi)$  is the loading capacitor.  $R_s$ ,  $R_m$ , and  $C_0$  are the electrode resistance, motional resistance and parallel capacitor of the resonator, respectively.  $C_\pi$  is the input capacitance of  $T_1$ . In order for the oscillations to take place, the negative resistance must be larger than the effective resistance of the resonator. A larger amplitude and therefore good phase noise can be obtained by using a small capacitor  $C_2$ . However, according to Eqn. (2) a small  $C_2$  will increase the effective resistance  $R_e$  which in turn reduces the amplitude. So the capacitor  $C_2$  as well as the bias current  $I$ , transistor  $T_1$  area, and the  $C_1$  and  $C_2$  capacitor ratio are optimized in order to achieve good phase noise. The resonator operates in parallel mode between the series and the parallel frequencies. The oscillation frequency is given by

$$f_0 = f_r (1 + C_m / 2(C_0 + C_L))^2 \quad (3)$$

where  $f_r = 1 / 2\pi \sqrt{L_m C_m}$  is the series resonance frequency of the FBAR, and  $C_m$  and  $L_m$  are its motional capacitor and inductance, respectively. Knowing that the motional capacitance  $C_m$  is very small

compared to  $C_0$ , the oscillation frequency is mainly fixed by  $f_r$  of the resonator as noted from the above equation. The oscillation frequency depends also on the loading capacitor  $C_L$ , so it can be tuned slightly by using a varactor in series with the resonator. The tuning sensitivity or the sensitivity of the oscillation frequency to the load capacitance variation can be expressed as

$$S = -f_r C_m / 2(C_0 + C_L)^2 \quad (4)$$

For the 5GHz FBAR used here, the capacitances  $C_m$  and  $C_0$  are in the order of fF and pF, respectively. So the tuning sensitivity is in the order of 70MHz/pF and is not sufficient for covering a wide bandwidth. Nevertheless, a varactor can be added in series with the resonator to compensate the technological variation of the resonator resonance frequency  $f_r$ . The sensitivity can also be adjusted during the design process by the resonator area which determines the capacitance  $C_0$ .

The micrograph of the chip is shown in Fig. 17.5.3; it occupies a silicon area of 640×650µm<sup>2</sup>. The resonator area is 170×200µm<sup>2</sup>. The active circuit and the ground line, made with the top metal layer (M4) of the BiCMOS process, have intentionally been kept away from the resonator to prevent any possible coupling with the FBAR. In the future, and after verifying the fact that bringing the ground line and active elements closer to the FBAR would not lead to the appearance of negative effects, one could further reduce the silicon area of the oscillator.

Phase noise has been optimized using Spectre RF. The core oscillator draws 1.7mA from a 2.7V supply voltage. The buffer amplifier consumes 3mA. On-wafer measurements were done to characterize the oscillator. The output spectrum obtained by the spectrum analyzer is shown in Fig. 17.5.4. The measured power is -8.4dBm. This is slightly lower than the expected value of -7.5dBm due to the resonator's lower Q factor. On-wafer phase noise measurement has been carried out using a delay-line discriminator technique. At 100kHz offset from the carrier, the achieved phase noise is -117.7dBc/Hz and is in agreement with the simulated value of -118.5dBc/Hz (Fig. 17.5.5). The corresponding figure of merit (FOM) [5] is -205.8. The simulated and measured performance of the FBAR oscillator are summarized in Fig. 17.5.6.

A 5GHz FBAR oscillator was designed using AMIS SiGe 0.35µm BiCMOS process and above-IC processing. Good phase noise performance was obtained. The FOM of the oscillator is approximately -206, which is better than those of state of the art integrated LC VCOs [3]. To compensate for process variations of the resonance frequency of the FBAR resonator, a varactor can be added in series with the resonator. The oscillator can be used as a reference signal source followed by a programmable divider for a completely integrated multimode PLL as well as a fixed RF oscillator for wide-band IF double conversion receivers. It can also be used in wireless sensor applications. The low silicon area of the FBAR oscillator and its good phase noise performance in combination with RF FBAR filters above-IC integration will certainly allow the realization of small form factor and low power completely integrated systems.

## Acknowledgements:

We would like to thank AMI Semiconductor for the active IC fabrication, CEA-LETI and CSEM for the above-IC processing of FBAR resonator. This work is supported by EC under Martina project.

## References:

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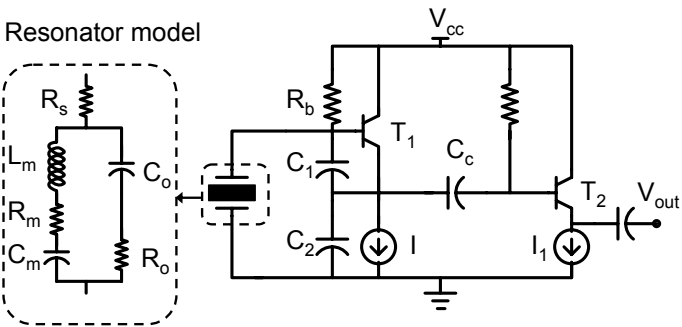


Figure 17.5.1: Oscillator schematic.

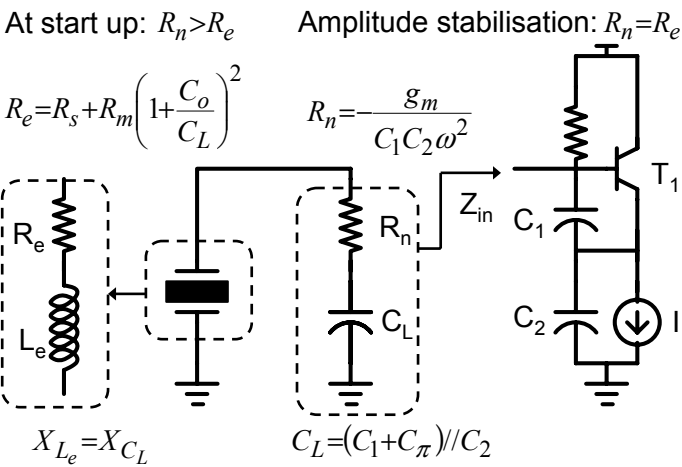


Figure 17.5.2: Oscillator equivalent circuit.

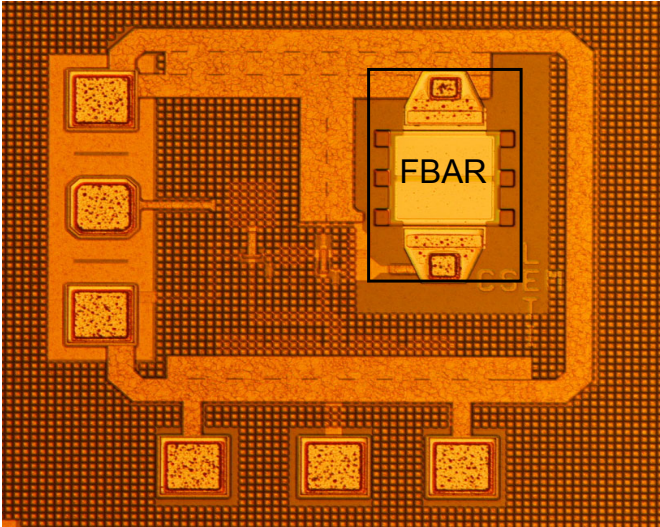


Figure 17.5.3: Chip micrograph.

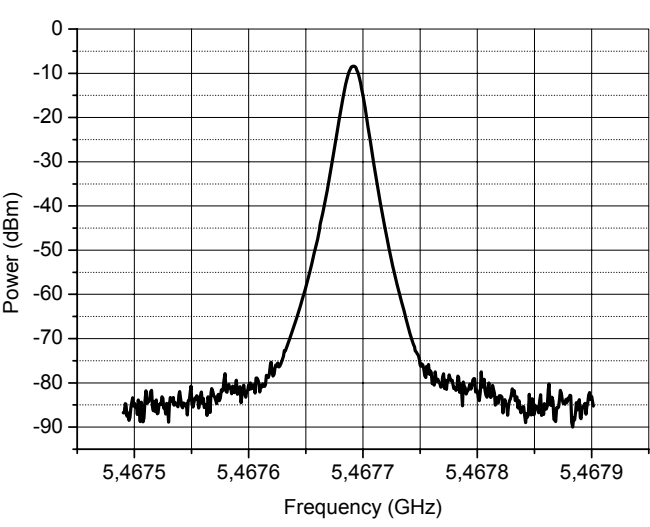


Figure 17.5.4: Output power spectrum.

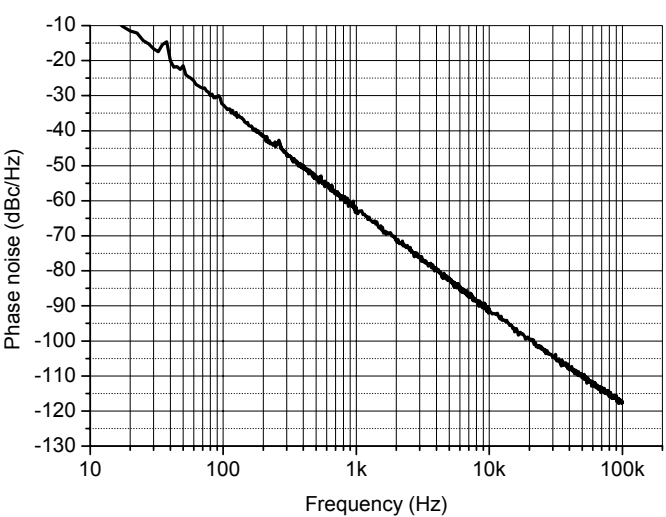


Figure 17.5.5: Phase noise.

	Simulation	Measurement
Frequency (GHz)	5.32	5.46
Output power (dBm)	-7.5	-8.4
Phase noise (dBc/Hz) @ 100kHz	118.5	117.7
FOM	206.4	205.8

Figure 17.5.6: Summary of oscillator performance.